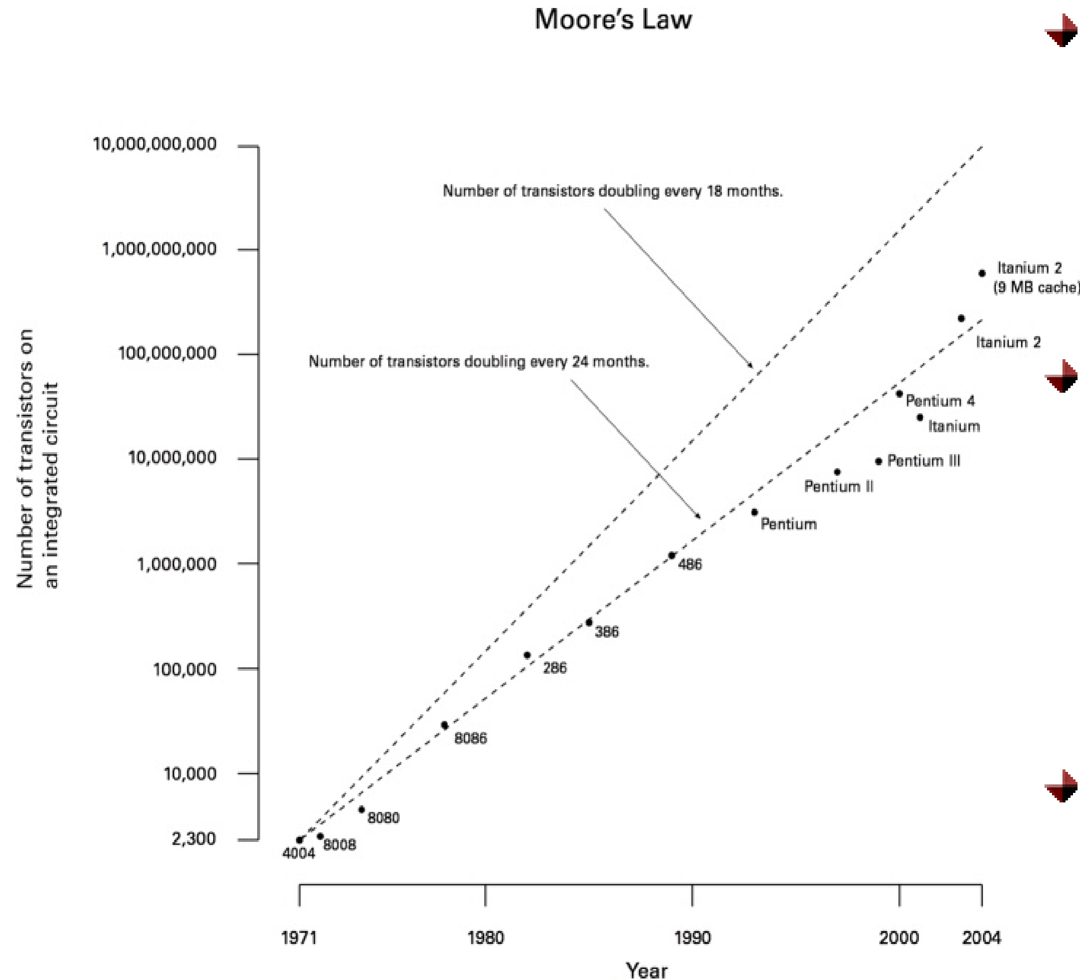
An overview of the trends and the challenges in RFIC Integration

Theodore Varelas
(t.varelas@thetamicro.com)
General Manager
Theta Microelectronics
Athens Greece

Outline

- Motivation
- Market drivers for single chip transceiver
- RF Integration Challenges and solution trends
  - Front-End Integration
  - Multi-mode integration
  - Integration with the baseband
  - RF SoC Design and Methodology
- Conclusions
- Q&A

Motivation



- **Discuss the trends and challenges of single chip radio frequency integration**
- **An overview of current solutions and today challenges to keep up with Moore's law in RFIC integration**
- **Engineering Innovation overcomes the RFIC integration challenges**

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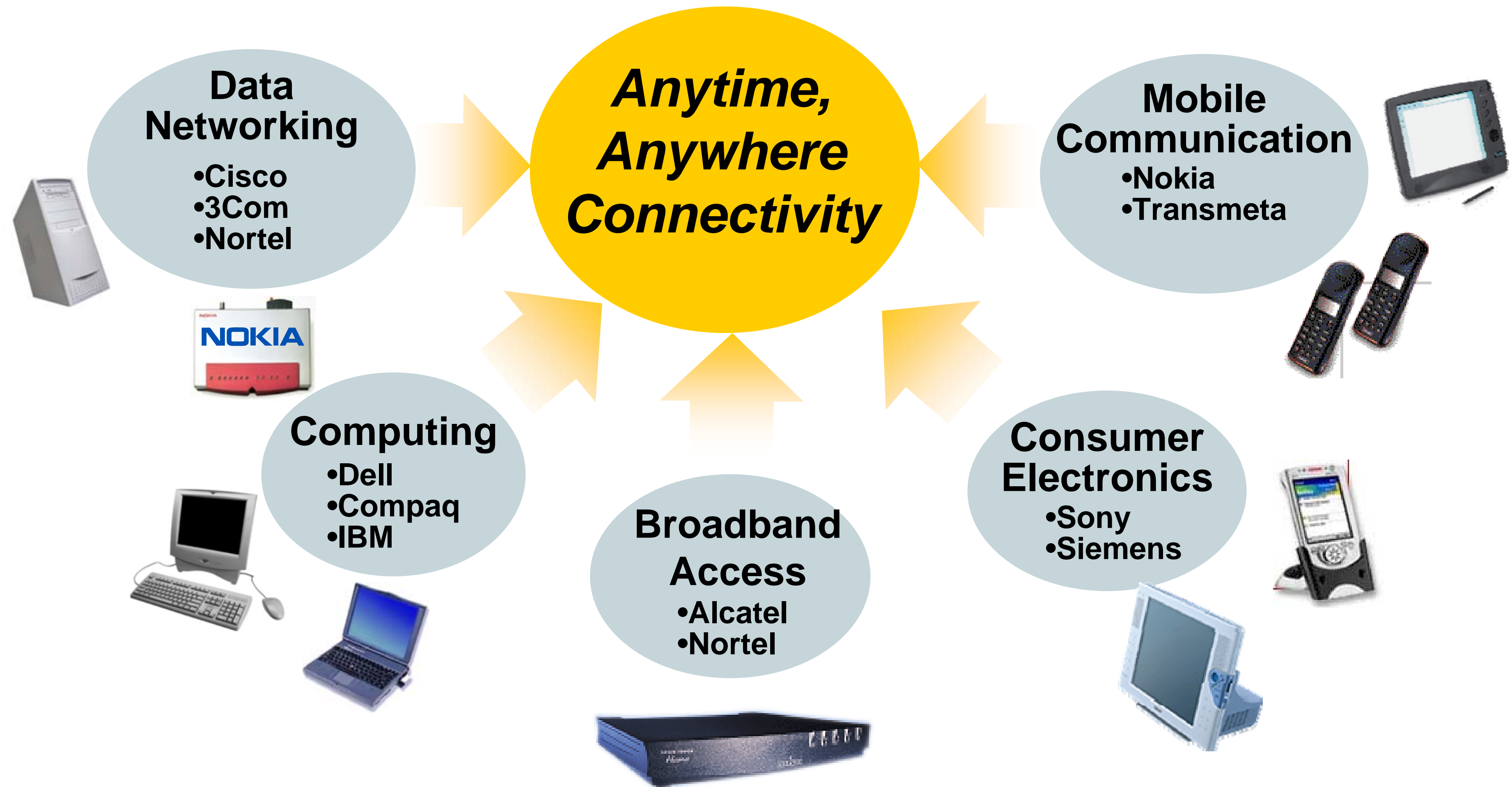
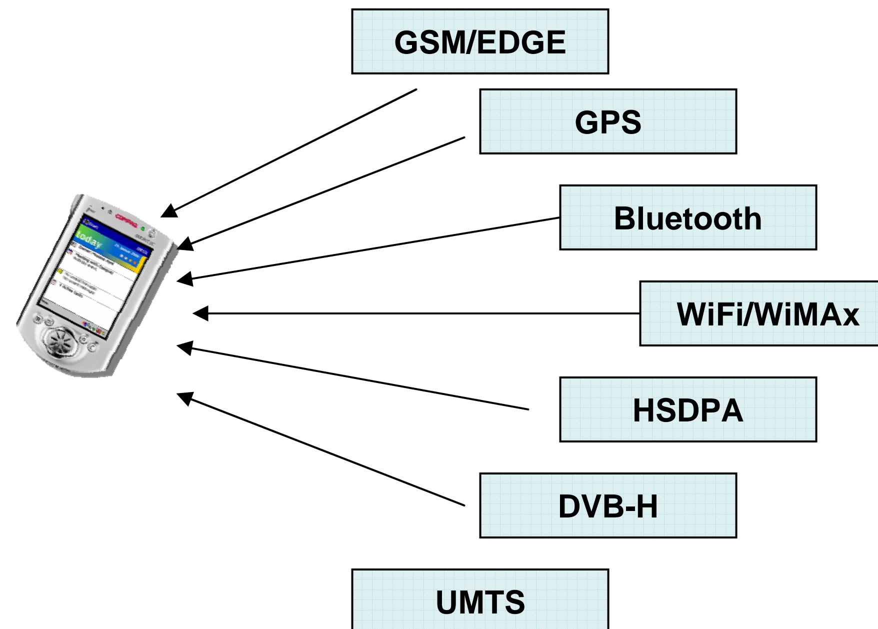
Broadband Wireless Data Connectivity



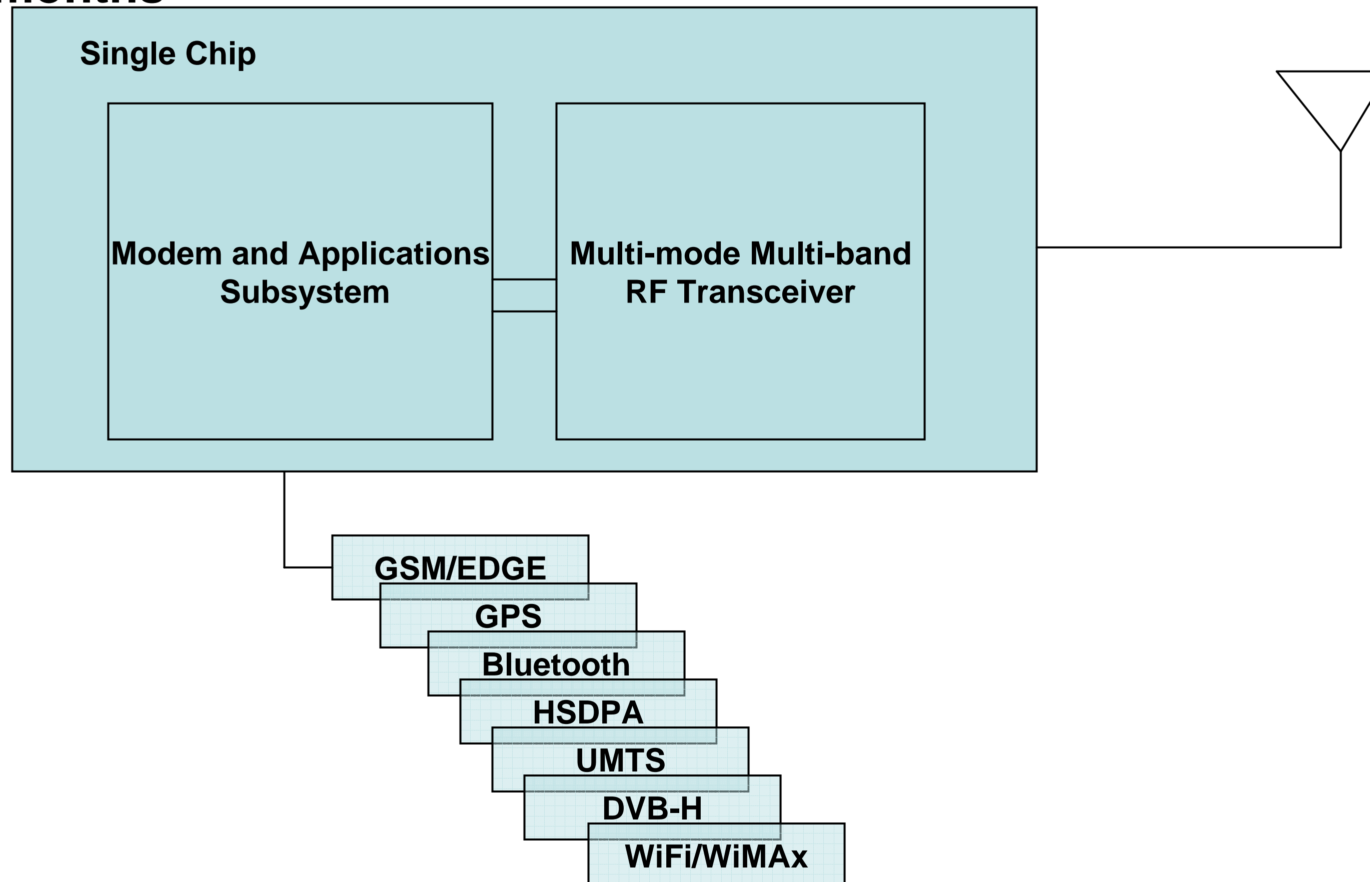
Market Trends

- Wireless anywhere, anytime, and any device as users continue to embrace mobility
- Mobile devices become ``All-in-One`` solutions

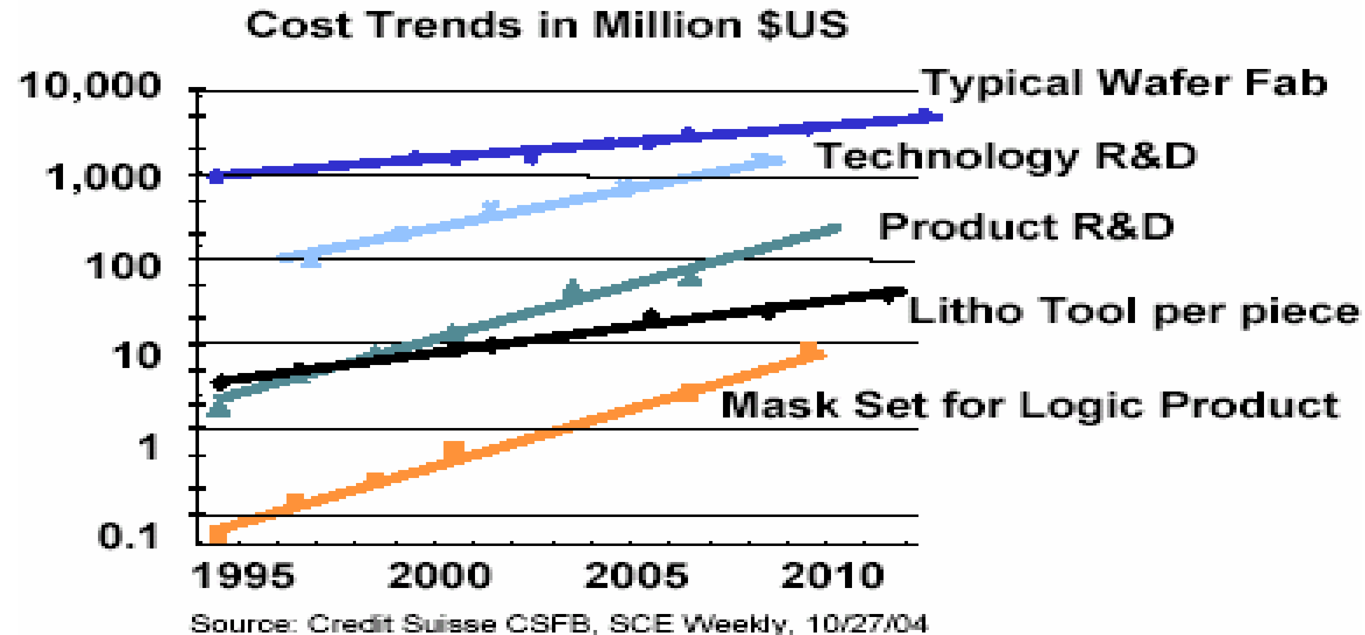


Mobile Radio Modem

- Functionality increases, while average selling price stays drops
- Integration of more functions on a single chip makes low ASP possible, consumer cycle need product development in less than 6 months

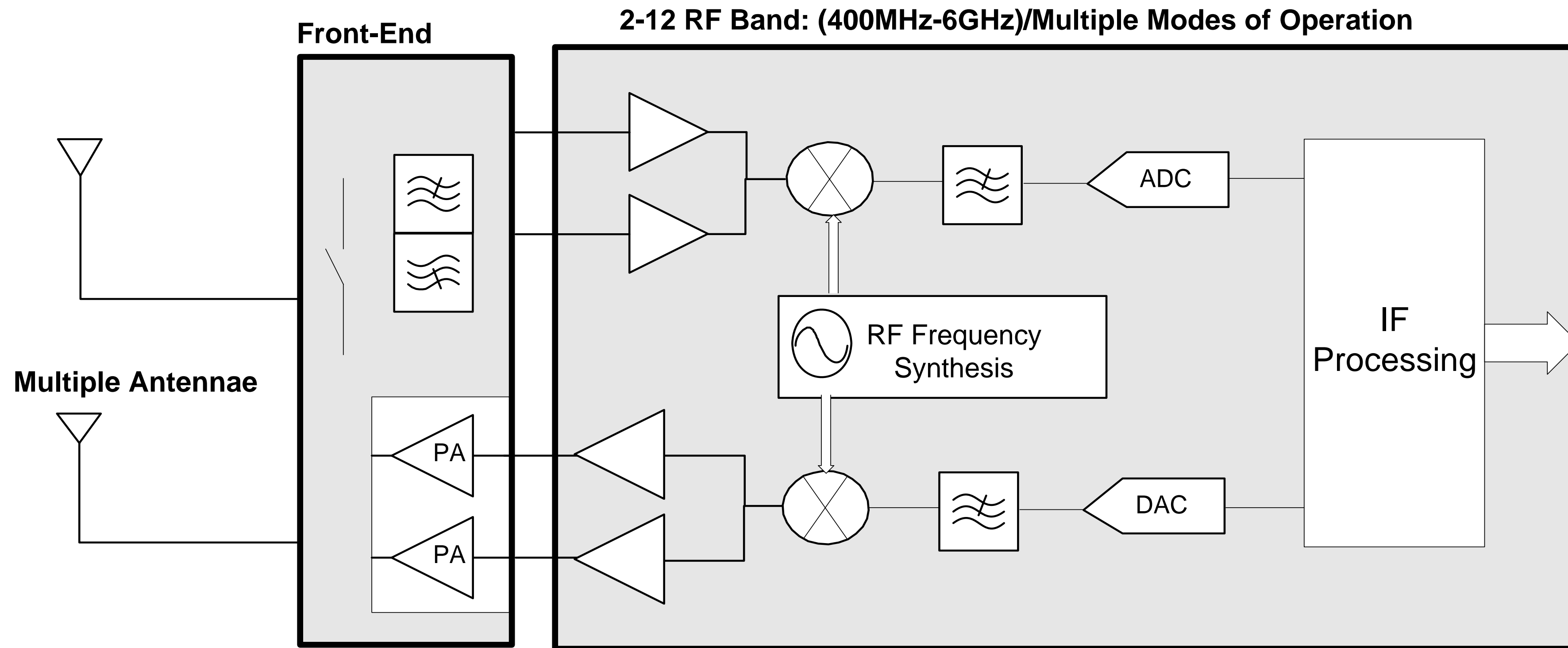


The cost challenge



- **Mask cost increases rapidly**
- **First pass RF design is a key objective for the engineering community to meet cost and time to market challenge**
- **How can RF design techniques meet the challenge**

RF Transceiver Unit



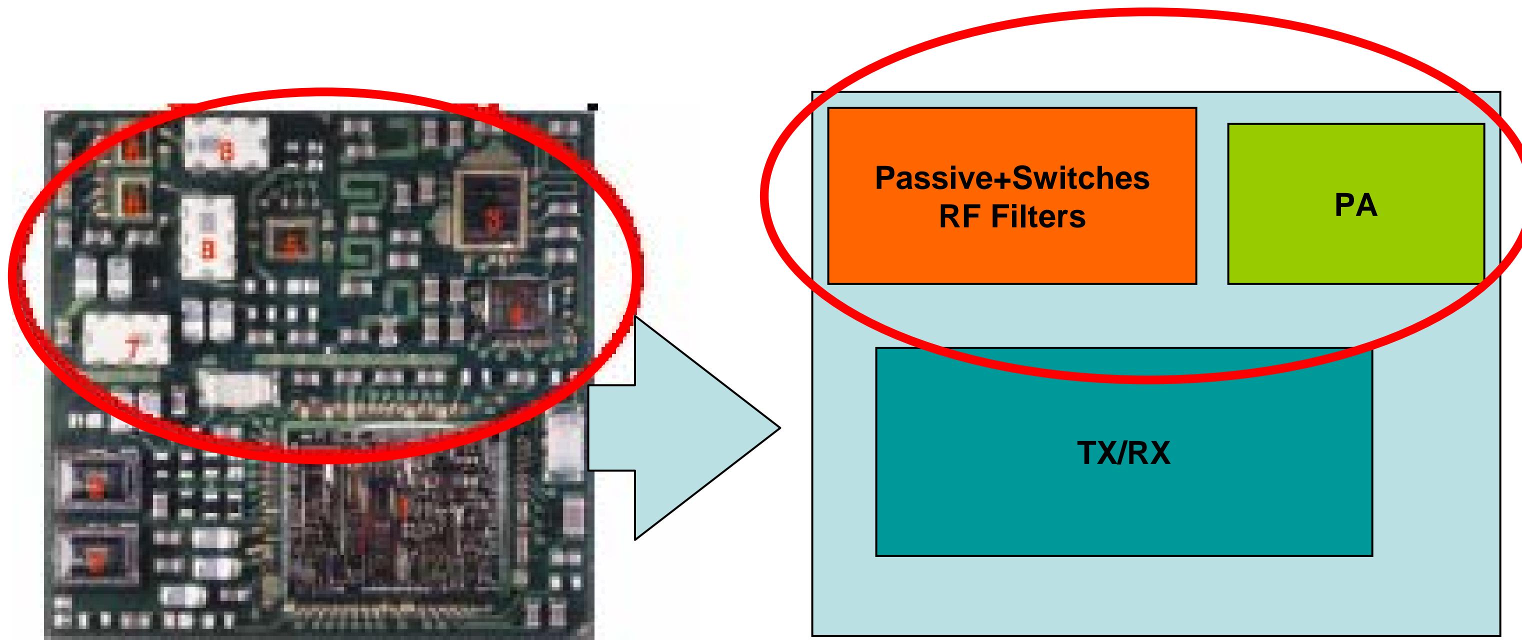
A typical RF Transceiver Unit

Front-End Integration

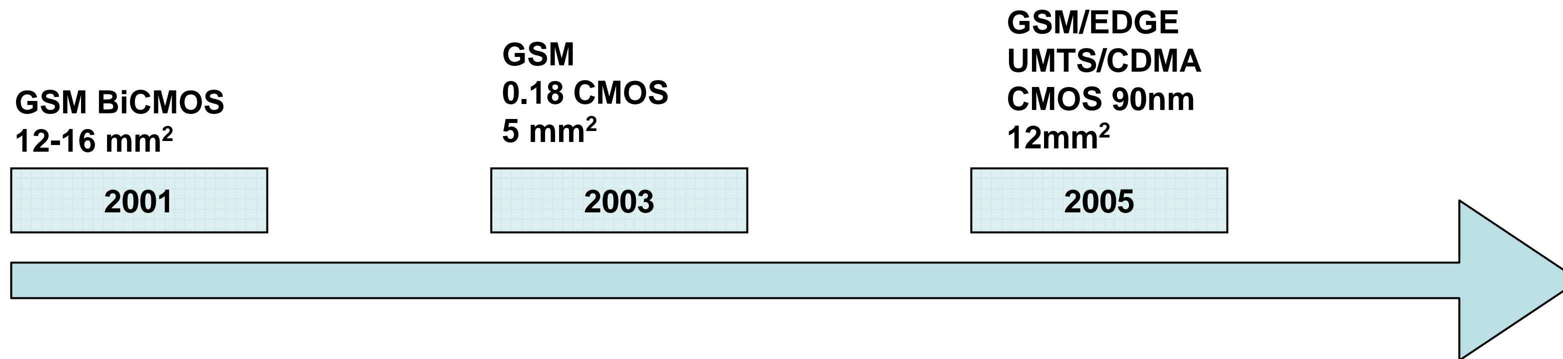
- **Cover frequency bands from 400MHz up to 6GHz**
- **Selectivity requires high-Quality factor RF-MW filters to be integrated in one package to meet cost and space requirements**
- **Integrate high performance Power Amplifiers and complex RF switching requirements**
- **Silicon in a Package Module addresses the challenges as it integrates chips and passive components, probably the best way to go as it allow us to marries the best from different technologies**

Typical SIP integration

- Module substrate incorporate all interconnects solder free
- SiP miniaturizes complex multi-band RF Front_Ends



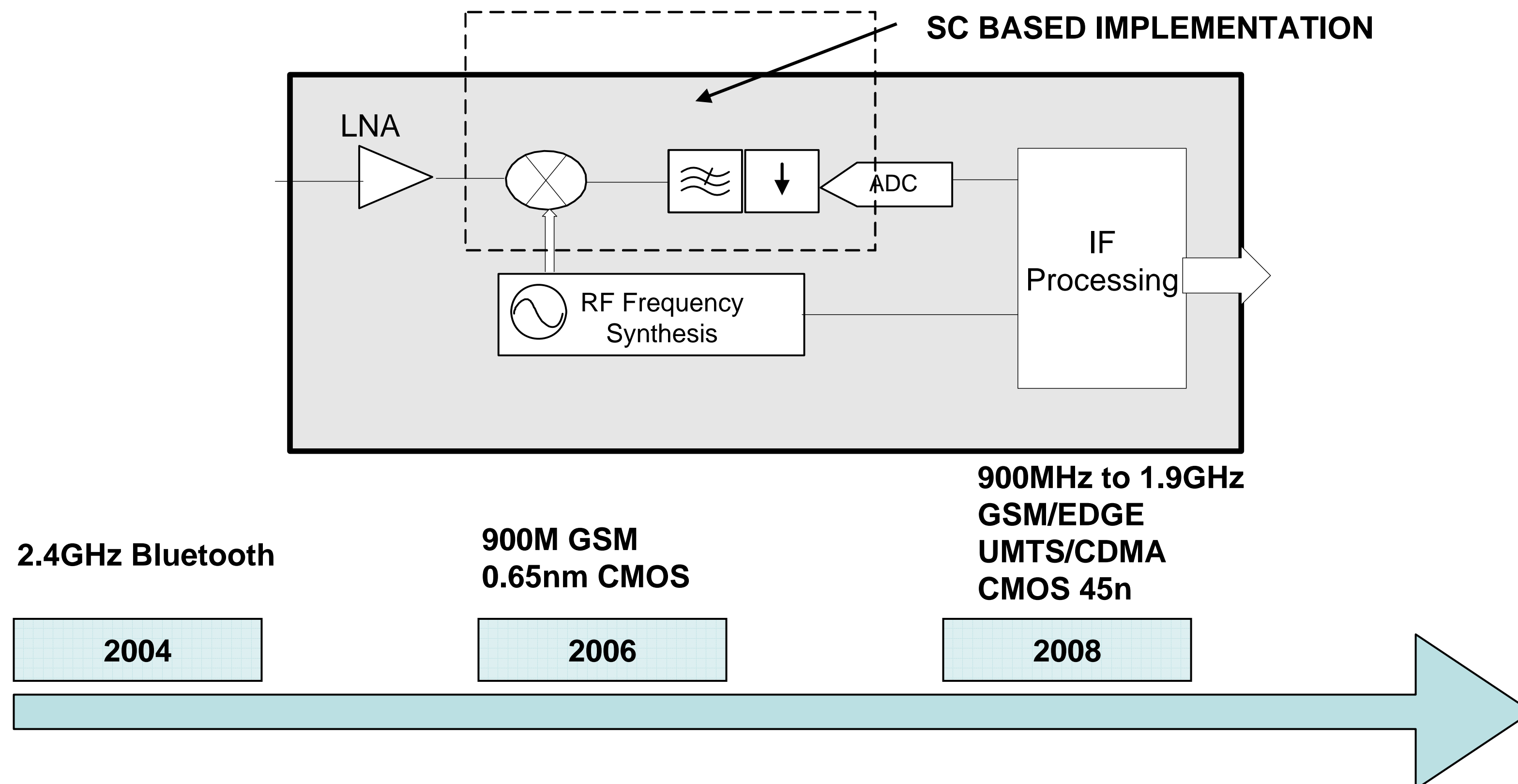
RF Scaling Challenge



- **RF and Analog Design does not scale as digital design**
  - **Passive, (inductor and capacitors) do not scale at the rate of MOS devices**
- **Integrating more RF functions costs in die size**
  - **An inductor at 65nm costs 300K gate**
- **Innovation always overcomes the barriers by leveraging new circuits and radio architecture solutions**

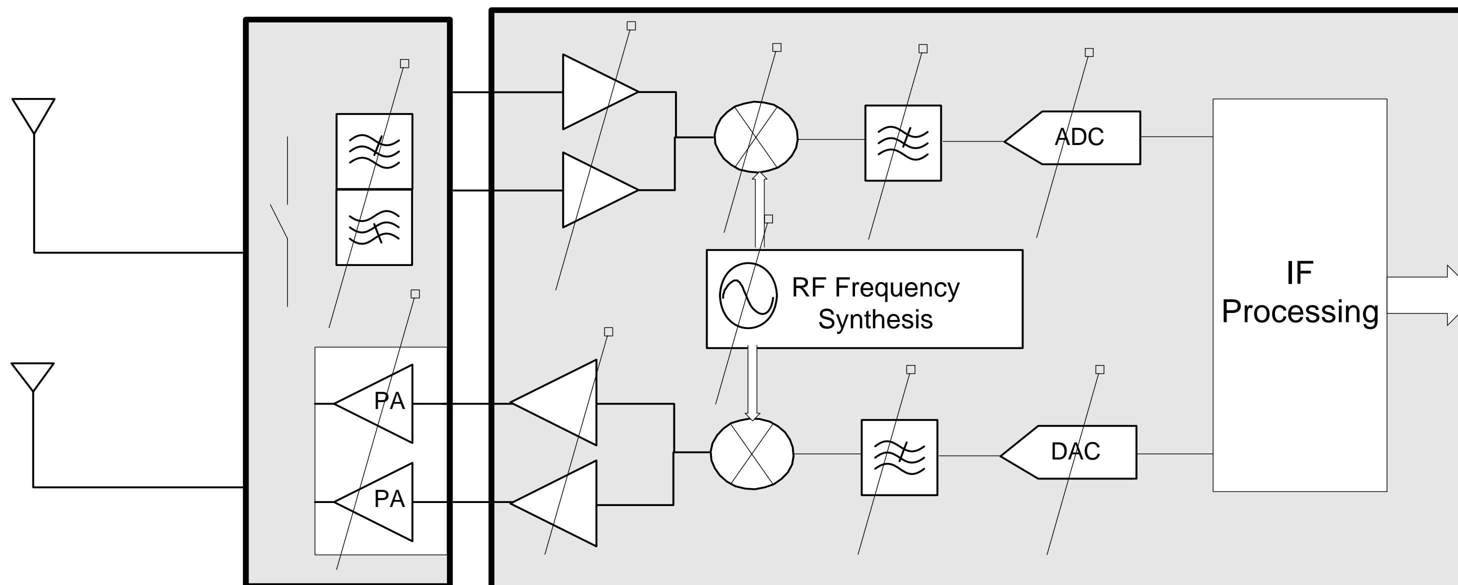
Innovation Example

- Discrete Time RF signal processing
  - Leveraging the nm-CMOS switching speed to enable discrete time domain based receiver and transmitter applications
  - PLLs are based on LC based Digital Controlled Oscillators



Multi-mode Multi-band

- Share functions and circuit resources key challenge for system architecture and circuit design
- Reuse circuitry between different operation modes and/or protocols while maintaining performance, power consumption and ***cost***



RF SoC Design Challenge

- Complexity surpasses the tool capability to verify performance
  - PA and VCO integration requires simulation engines to co-simulate Electromagnetic phenomena while predicting electric behavior
  - Verification and post-layout simulation complexity increases as new coupling mechanisms need to be addressed
    - Substrate couple between RF and High speed basedband processors
- Design Methodology and Simulation Methodology key to maintain development budget within reasonable limits
  - 90nm mask cost, 65 nm mask cost
- Cad tool engineers will meet the challenge

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Conclusions

- **Wireless connectivity proliferation into consumer products introduces new cost and time to market requirements for the RF IC design**
- **The level of integration along with performance challenges poses a continuous challenge for the RF design community**
- **Innovative approach in RF IC architectures, design and CAD tool solution are addressing the challenge**

Thank you
Questions?